# Project description:

## Background

### State of the art:

One of the hottest topics in condensed matter physics is the realization of a quantum computer. The main advantage of such a quantum computer would be its ability to solve specific classes of algorithms orders of magnitudes faster than classical computers. A classical computer is based on deterministic two level states called bits. A quantum computer is also based on two level states (basis states) called quantum bits (qubits). However, a qubit unlike a classical bit exploits the quantum effect of superposition. As a consequence, a quantum system can be simultaneously in both basis states.

There have been several proposals for implementing such a qubit, with just some solid state realizations listed below:

* Electrons on Helium (He) [1]
* Semiconductors:
  + - Nuclear spin qubits [2]
    - Electron (hole) spin qubits [3]
* Superconductors:
  + - Flux qubits [4]
    - Charge qubits [5]

One of the above mentioned suggestions, which came in 1998 by Loss and DiVincenzo, was to use the spin of electrons (holes) for the realization of qubits. The spin, an intrinsic quantum mechanical property of every elementary particle, lifts the degeneracy of an orbital energy level in the presence of an external magnetic field. The orbital level splits into two, typically labelled as spin-up and spin-down. This two level system can then act as a qubit, the so-called spin qubit.

However, for creating and manipulating the spin qubit, one must first confine the charge into a region, which is in size comparable to the charge particle wavelength. Such a confinement can take place in a structure called quantum dot (QD). QDs are very small structures (their diameters can reach tens of nanometers) and because of their almost zero dimensionality, the energy levels for a charge particle are discrete and far away from each other.

Not every two level system can create a useful qubit for the realization of a scalable quantum computer. In 1998. DiVincenzo published a list of conditions which a qubit should fulfill for a quantum computer to work correctly [7]:

The 5 necessary criteria are:

* **The qubit should be well-defined:** A well defined qubit is a two level (two state) system whose levels are distinguishable and highly controllable.
* **It should allow reliable state preparation:** The qubits needs to be deterministically driven into the initial state so that the next computational step can take place**.**
* **It should show low decoherence times (long coherence times):** Because of the several noise sources to which the qubit is exposed its initially prepared state is lost (it does decohere) with time. It is desirable to have as long as possible coherence times.
* **A “universal” set of quantum gates (state manipulation) should exist:** In the classical logic the Boolean function set (set of gates) is functionally complete or universal if any other function (gate) can be represented by it. The same functional universality applies for the quantum logic. *(I think I can say it like this, but I did not find it directly said like that anywhere)*
* **A qubit measurement capability (state readout) should exist:** After a several state manipulations have been applied to the qubit, one should be able to read the computed result, it’s quantum state.

**For all type of qubits there is battle between the manipulation time on one side and the coherence time on the other side. This is so because performing quantum computation, many single operation need to be done before system decoheres. The benchmark for the manipulation time is the minimum time needed for going from one state to the other.**

**For the spin qubits, which this proposal deals with, different materials have been investigated aiming to find the material with the highest coherence vs manipulation time ratio.**

**Materials**

Silicon **(Si)** has emerged as a promising material for the realization of spin qubits because it can be isotopically purified and left just with the 28Si isotope which is a zero nuclear spin element. Thus the nuclear noise can be eliminated and the coherence time boosted in comparison to the broadly used gallium arsenide (GaAs). The additional big advantage of Si is its compatibility with current CMOS technology. This could become very important when moving towards the realization of a large number of qubits as required by quantum algorithms.

There are several approaches of defining QDs in silicon.

One way is by means of a phosphorous (P) dopant. In that case a P atom behaves as an electron QD because of its confining potential. Andrea Morello’s Group from the UNSW in Australia, by applying the spin echo pulse sequence, has measured electron spin coherence time T2ECHO exceeding 200 microseconds, in a non – isotopically purified Si:P system, while the duration of one full spin rotation in this case was τπ = 75 ns [3]. By using isotopically purified 28Si:P samples and the nuclear spin of a P atom as a qubit, the same group has achieved nuclear spin coherence time of T2ECHO = 60 milliseconds using spin-echo technique and duration of τπ = 50 μs [2].

M. Veldhorst et al. by using lithographically defined electron QDs in Si have measured spin coherence times using the CPMG pulsing technique of T2CPMG = 28 ms and τπ = 1.5 μs [17].

Finally, E. Kawakami et al. by using a single-electron QD in a Si/SiGe heterostructure qubit, have measured T2ECHO = 40 μs, while τπ = 0.15 μs [18].

One limitation of Si is the difficulty to perform fast gate operations while maintaining the good coherence. One way around this problem is to use the spin-orbit interaction of holes and perform spin manipulation via electric fields (as described in more detail in the *Spin manipulation measurements* section). Using this approach R. Maurand et al., realized very recently the first CMOS spin qubit by using a hole confined in a transistor made out of p-type Si. The reported T2ECHO time was 245ns and τπ ≈ 3 ns. [11].

Holes in germanium (**Ge)**, on the other hand, have much higher spin orbit coupling which should allow much **faster spin manipulation times**. In addition, for purely heavy-hole (HH) states the dephasing time should be very long [21].

In our group we study qubits, in Ge self-assembled nanostructures [10], which are created by epitaxial growth of Ge on Si. Such a growth can lead to various types of nanostructures. In this project the so-called Ge hut-wires are going to be studied. Very recently magnetotransport measurement have shown that holes, in this type of structures, are of the HH character, suggesting long coherence times for this material system.

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Figure 1: Stability diagram of a SiGe nanowire single QD (left). Scanning electron micrograph of SiGe nanowire contacted by palladium Pd source and drain electrodes (right) [10]

**Measurement techniques:**

Different type of measurement techniques have been used in order to extract the state of a spin qubit and its coherence time:

* DC current readout: The DC current readout is sensing the electron transport through the qubit by means of current measurement. It is prone to low frequency 1/f noise and the bandwidth (BW) is low because of heavy filtering necessary for achieving low effective electron temperatures.
* Differential measurement (AC current readout): The differential measurement (AC current readout) has the same drawbacks as DC current readout. It is typically done with a low frequency lock in technique. Because of the low frequency noise, a lock in amplifier usually operates on a very narrow BW around the measurement frequency, which leads to long measurement times.
* Ohmic reflectometry: Ohmic reflectometry is a technique which indirectly senses the impedance change of a QD by monitoring the amplitude or phase of the reflected from the QD wave (see Figure 2 for a more detailed explanation). It is usually performed by high frequency lock-in techniques and is not prone to 1/f noise.
* Gate reflectometry: Similar to the ohmic reflectometry but it is connected to a gate and not to the source or the drain lead. **It’s big advantage is that it does neither require charge transport through the QD hosting the qubit nor the existence of a charge sensor.**

**Explanatory box: What is reflectometry?**

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Figure 2: Basic principle of ohmic reflectometry. Resonant circuit is consisting of the SHT sample and matching circuit. SHT sample is represented with parallel combination of CS and RS. S and D denote the source and drain contacts of the SHT, respectively. The matching circuit formed with an inductor L and a capacitance C is connected to the source contact.

Reflectometry is a readout technique based on the change of the wave reflection coefficient Γ. It comes from the electromagnetic wave principle – if a wave is travelling in a media with impedance Z0  (e.g. coaxial cable) and it encounters a change of impedance from Z0 to Z (e.g. end of coaxial cable), a portion of the wave will be reflected back according to the expression: , where Ar is the amplitude of the reflected signal, Ain the amplitude of the incoming wave and Γ is the reflection coefficient.

By using a resonant circuit (matching circuit with an incorporated SHT) as showed in Figure 2, instead of the open end of a coaxial cable one can make use of the information contained in the reflected wave amplitude. For achieving this, the elements of the resonant circuit, the inductance L and the capacitance C needs to be chosen to achieve the matching condition on the resonant frequency of the circuit, . Matching condition is the situation in which the typically large resistance (~100 KΩ) of the SHT is transformed, by the inductor and capacitor, to near 50 Ω. This value is the characteristic impedance of the RF line Z0, thus the wave reflection coefficient Γ is minimized. In that case sensitivity is maximized [13] and small changes in the SHT impedance results in an observable change in the reflected wave amplitude.

Thus, if a hole tunnels -> SHT impedance changes -> Γ changes -> amplitude and phase of the reflected wave changes.

### Definition of the problem:

**Since charge transport through the QD hosting the qubit, is in many qubit experiments unwanted because it is an invasive method, alternative methods have been looked for.** A usual solution to this problem is to place, next to a measured qubit, an additional, separated QD in the form of a single electron (hole) transistor or a quantum point contact, called charge sensor. The charge sensor is electrostatically coupled and thus sensitive to the charge configuration in the qubit. The charge sensor itself is well coupled to ohmic contacts thus it is suitable for charge transport measurements (DC current readout, AC current readout) and ohmic reflectometry.

**However, charge sensors suffer from thermal broadening of the conductance features (coulomb peaks, conductance plateaus) which lowers the sensitivity and thus the readout speed. In addition, their gate voltage needs also to be continuously adapted in order to compensate the influence of the qubit gates on their conductance. Finally, by looking into the future, for the realization of a usable quantum processor, the qubit number needs to be drastically scaled up. Adding charge sensors next to each qubit will lead to additional complexity.**

**Gate reflectometry does not suffer from the previously listed problems.**

By connecting the gate electrodes defined for creating and tuning a double quantum dot (DQD) in GaAs/AlGaAs heterostrucure to a lumped element resonator acting as a gate reflectometry circuit, J. I. Colless et al. achieved a charge sensitivity of 6.3 meHz-1/2 (smaller is better) [14]. Last year, M.F. Gonzalez – Zalba et al. reported an improved charge sensitivity of 37 μeHz-1/2 by using the similar gate reflectometry approach for a silicon nanowire based DQD device [12]. The reported sensitivity is similar to that achieved with ohmic reflectometry in charge sensors such as 1 μeHz-1/2 for RF quantum point contact and 100 μeHz-1/2 for RF single electron transistor [12].

High sensitivity and thus high speed of the gate reflectometry circuit is desired for performing spin state measurements in the single shot regime. Also it is desired for capturing fast stability diagrams (which usually can take up to several hours using DC or AC current readout techniques) and thus performing the measurements much faster.

### Proposal objectives:

The objectives of this proposal are to **design a** **fast gate reflectometry** system which will be used in order to study in second part of my PhD thesis the spin properties of the Loss-DiVincenzo qubit created in a Ge- based, DQD.

For the gate reflectometry, the goal is to achieve a charge sensitivity comparable or even faster than the one reported in [12]. That will allow us to have a high bandwidth system necessary for the qubit read out. After the gate reflectometry will have been set up the focus will go to the realization of the Loss-DiVincenzo hole qubit in a DQD structure. The first measurements to be performed are the ones for determining the spin relaxation time T1 . Subsequently experiments in order to investigate the coherence time of the qubit are going to be performed. More concretely, spin manipulation experiments for measuring the spin dephasing time T2\*, the spin coherence time using spin echo technique T2ECHO, and the spin coherence time using the CPMG (Carr-Purcell-Meiboom-Gill) pulse sequence technique T2CPMG, are going to be conducted.

### Working schedule:

#### Designing initial version of reflectometry setup: sample holder, readout circuit, instrumentation setup

**Sample holder**

In order to tune the gate reflectometry system, measurements will be initially performed at 4K, by using a single QD device as SHT. During the first year of my PhD I have already prepared a 4K dip stick (Figure 3) for such reflectometry measurements. Particular attention was paid to the sample holder, fabricated out of a printed circuit board (PCB). DC electrical signals are sent to the sample through low thermal conductive wires twisted in pairs finishing in a PCB connector; radio frequency (RF) signals are sent through the coaxial cables. The DC signals are low pass filtered with surface mounted RC filters (Figure 4) to reduce thermal noise from the wires. After low pass filtering, the DC signals are routed to the gold plated bonding pads around the area in the middle of the PCB (sample area) on which a typically 5x5 mm sample is glued with silver paste (Figure 4). The RF coaxial lines are finishing on the PCB mounted SMP connectors. After the SMP connector, a DC signal is added to the RF signal by using a bias tee. From there the signal is routed to the PCB bonding pads. Electrical contacts from the PCB bonding pads to the sample bonding pads are achieved by wedge wire bonding.

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Figure 3: Plexiglas 4K dip-stick used for cooling down samples to 4K and performing reflectometry measurements. The left picture shows the whole stick, while the right is a zoom-in, highlighting the directional coupler and the low noise Minicircuits ZX60-33LN-S+ RF amplifier. An additional low noise cryogenic RF amplifier CITLF2 from Sander Weinreb’s Caltech Microwave Research Group can be added in order to increase the SNR of the measured signal.

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Figure 4: Initial version of the PCB sample holder. The left figure show the upper view of the PCB board while the right figure focuses on the back side.

**Resonant Circuit**

The used resonance circuit consisted of a matching circuit (Figure 4) and the SHT. SHT is schematically presented as resistance RS in parallel to the capacitance CS, as can be seen in a simple circuit model in Figure 2. For the matching circuit, the surface mounted inductor Murata 1.2 μH and the varactor MACOM MA46H070-1056 were used. The Varactor – a voltage tunable capacitor - was used in order to be able to always achieve a good matching condition despite the change of the SHT resistance Rs [13], as explained in “What is reflectometry” section of the “State of the art” chapter.

For performing the ohmic reflectometry measurements the RF signal was sent down the coax line (Figure 3, right) towards the QD device. The signal which gets reflected from the resonant circuit is sent via the directional coupler to the amplifiers. The amplifier configuration, shown in Figure 3 (right), is used to preserve the signal to noise ratio (SNR). After the sample, a very low noise cryogenic amplifier, Weinreb’s CITLF2, is used to amplify both signal and noise by the same amount (around 20 dB), adding a very small amount of itself noise, thus almost equalizing the SNR on its input with SNR on its output. Higher noise level on the output of the CITLF2 amplifier allows the second, noisier amplifier to achieve SNR on its output approximately same as the SNR on its input. Such an amplifier chain enables non – degrading propagation of the SNR from the sample stage to the higher noise room temperature.

**Instrumentation setup**



Figure 5: Simplified schematic of the overall measurement circuit

For conducting the measurements several instruments have been used.

* Reflection coefficient measurement: vector network analyzer (VNA) from Rohde and Schwarz, model ZNB20
* DC biasing of the single hole transistor: auxiliary bias outputs of a Stanford Research SR830 lock-in amplifier
* DC current measurements: current amplifier from Stanford Research SR570
* For attenuating the RF signal sent to the sample: Minicircuit’s attenuator
* For amplifying the reflected from the sample RF signal: series of Minicircuit’s and CITLF3 low noise amplifier
* Instrument control and data retrieval to the PC: Python application.

#### Germanium nanowire based, hole spin single QD tuning and characterization with the initial version reflectometry setup



Figure 6: 3D model of a silicon germanium nanowire-based single QD sample SHT, designed by H. Watzinger. A single QD which confines holes is formed in the nanowire beneath the gate (green).

The single hole transistor sample was fabricated by H. Watzinger and the nanofabrication description can be found in [10].

Using the setup described in the previous chapter, the SHT (single QD) formed in the germanium hut-wire (Figure 6) was tuned in the Coulomb blockade regime applying DC voltages on source, drain and gate electrodes (Figure 5). Charge stability measurements were conducted in the Coulomb blockade regime showing a Coulomb diamond pattern. A Comparison of the DC current and ohmic reflectometry measurements has been done. The DC current was measured by applying a bias on source and reading the current from drain contact (Figure 5), while for the reflectometry measurement the LC matching circuit was connected to the SHT source contact (Figure 5).



Figure 7: Comparison of the DC current transport (left) and the ohmic reflectometry (right) measurements for the SHT in a Ge hut-wire.

By adjusting the integration time to be similar for both measurements, it can be seen that the reflectometry technique enables us to see more features like the excited orbital energy states of the SHT (Figure 7).

We have compared our reflectometry setup with the one of D. J. Reilly et al. for which they reported conductance sensitivity of 5\*10-6 e2/h Hz−1/2 by performing reflectometry on a quantum point contact in a dilution fridge with electron temperature of 120 mK [19].

By using the same methodology as in [19] for characterizing the reflectometry setup we have measured a just around five times lower sensitivity despite the much higher temperature of 4K. This is a quite good when considering that the thermal broadening of the energy levels at 4K, leads to much wider coulomb peaks. Such results in a much smaller resistance change for a small gate voltage modulation and thus a smaller sensitivity

#### Second generation of the reflectometry setup

The first generation of the used setup and PCB board aimed to verify that indeed we have the knowhow to perform RF reflectometry measurements. The second generation of the reflectometry setup will be installed in dilution fridges allowing us to achieve temperatures down to 10 mK.

For the purpose of measuring several samples and due to the necessity for a higher number of RF lines dictated by experiments of spin manipulation, a new PCB will be designed. The new design will allow frequency multiplexing of four different reflectometry resonant circuits enabling the measurement of four samples by using just one RF line and amplification stage. We will install in the dilution fridge insert a similar reflectometry system like the one used in the 4K dip-stick. However there will be several improvements. There will be an upgrade in terms of using lower thermal conducting stainless steel cables, attenuators, and additional DC filtering of all the DC wires. In addition, a Niobium titanium superconducting cable is going to be used between the input of the cryogenic amplifier and sample stage because of its very low thermal conduction, to avoid heating of the mixing chamber stage of the fridge which has a cooling power of a few tens of μW in the insert.

The vector network analyzer which was used so far for the measurements will be replaced with a Zurich Instruments UHF lock in amplifier which enables faster and longer data acquisition, more inputs and generally more measurement flexibility. For the spin relaxation time and spin manipulation measurements, to be described below, arbitrary waveform microsecond pulses with a nanosecond rise time are needed. Those are generated using a Tektronix AWG5014C. The measurement will be - conducted using the QTLab measurement application developed in Python initially by the Delft Quantum Transport (QT) laboratory. We modified it according to our needs. All the codes can be found on the GitHub: <https://github.com/nanoelectronics-new/qtlab>

#### Moving towards gate reflectometry DQD_reflectometry

Figure 8. Gate reflectometry schematic on the Ge nanowire DQD sample, nanofabricated in our group. LC resonators are connected to the three gates. Because of different inductor values, resonance frequencies of three matching circuits above are different enabling so called frequency multiplexing technique.

As in the ohmic reflectometry also for the gate reflectometry the readout parameters are the phase shift ∆φ and the amplitude change ∆γ of the reflected signal due to the charge configuration change in the QD or DQD system. , , , where Q is the quality factor of the resonant circuit, Cp is the parasitic capacitance, Cg is the gate to dot coupling capacitance and CΣ is the overall QD capacitance [12]. The capacitance Cg can be approximated with that of a parallel plate capacitor since the gate electrode and the nanowire separated by a thin dielectric, form a capacitor. From the above expressions it can be seen that a higher coupling between the gate and the QD (higher Cg) leads to higher sensitivity of both ∆φ and ∆γ.

Using gate reflectometry in a gate defined GaAs DQD J.I. Colless et al., achieved charge sensitivity of 6.3 meHz-1/2, having Cg/CΣ ≈ 0.05 [14]. Using 1.9 nm HfSiON oxide as dielectric in a silicon nanowire field effect transistor, M.F. Gonzalez – Zalba et al. achieved a charge sensitivity of 37 μeHz-1/2, with Cg/CΣ = 0.92 [12]. For comparison, the sensitivity achieved using ohmic reflectometry and a rf-QPC (rf-SET) as a charge sensor is 100 μeHz-1/2 (0.9 μeHz-1/2) [12]. Thus the performance of gate reflectometry is very close to that of ohmic reflectometry. In our system using by using ~ 4nm HfO2 as a dielectric, which has εroxide = 24, we expect to have a Cg/CΣ comparable to that reported in [12].

*Optimizing the gate reflectometry*

From the equation for ∆φ, it is clear that there are two factors which are critical for getting a sensitive gate reflectometry setup. Firstly to **reduce the parasitic capacitance** **Cp** as much as possible by engineering the sample holder. Secondly, to **achieve high quality factor Q** of the resonant circuit.

For **reducing the parasitic capacitance Cp** coming from the coupling of the PCB RF lines and bonding pads to the ground planes, the Sonnet software can be used. Simulations of the PCB RF lines and bonding pads geometric capacitance in respect to their dimensions, routing configuration and PCB dielectric will be performed.

**Quality factor Q** dependence about different inductors and capacitors will be examined.

Additional losses in a gate reflectometry system are PCB dielectric losses, losses in PCB RF transmission lines [12].

Losses in the PCB dielectric will be addressed by using a dielectric with lower dielectric loss then the currently used FR4, e.g. some of the Rogers Corporation laminates.

The RF lines transmission losses come probably from the unwanted reflections due to the transmission line routing and splitting needed to connect more reflectometry readout circuits – frequency multiplexing. This assumption should be tested and the **optimum configuration of the PCB RF lines** could be achieved by using again the Sonnet software for simulating the RF line scattering parameters.

### Spin dynamics experiments

Once the gate reflectometry setup will be properly working, I will focus on performing spin manipulation experiments. During my PhD I will focus on the Loss-Divincenzo spin qubit.

*For achieving good state preparation, fast manipulation and fast measurement, additional mechanisms are required beyond ones offered by single QDs. One of the most promising building block for the realization of the spin qubit quantum computer based on QDs is a serial DQD system. A DQD system consists of two neighboring QDs tunnel coupled to each other, which simply means that they can exchange charge particles by tunneling. The*



Figure 9: Spin state readout based on spin blockade shown for gate defined DQD. The blue circles represents the individual QDs, the grey lines the gates and the black arrows in the QDs the electron spin direction in the left and the right dot.

main physical property which makes them favorable for the realization of a qubit is the Pauli exclusion principle. It says that two identical fermions (in this specific case electrons or holes) cannot occupy same energy state.

Figure 9 describes how spin blockade can be used to extract information about the spin degree of freedom in the left QD in the DQD system. If the spin configuration forms a singlet state S(1,1) (the numbers in brackets denote the hole number on the left and right dot respectively), like shown in Figure 9a, then after electrostatic pushing, by applying voltage pulses on gates L and R, the hole is allowed to tunnel to the right dot, forming a singlet S(0,2) state. In the case below, Figure 9c), holes in both dots have the same spin, forming a triplet T(1,1) state, and due to Pauli exclusion principle they stay in the (1,1) configuration after electrostatic pushing because the triplet state T(0,2) is too high in energy and thus not available.

##### Measuring the spin relaxation time T1

For measuring the spin relaxation time, an approach similar to the approach of Koppens et al. [20] will be used. The DQD will be tuned to a the (0,1)-(1,1)-(0,2) triple point. The left dot is initially empty while the right dot is populated with a spin in its ground state, a spin down hole. First, pulsing the gate of the left dot will bring its spin up and spin down energy levels above the Fermi level, μF, of the lead, allowing lead to dot hole tunneling (holes tunnel to higher lying electrochemical potentials). Since the tunneling is most likely spin independent, the left dot is loaded with a random hole spin from the lead, during the loading time tL. The double dot is thus in either a singlet (1,1) state or a triplet (1,1) state and is left in that configuration for the waiting time tw. After the tw, a second pulse level is applied in order to bring the hole from the left QD to the right QD. For an S(1,1) configuration tunneling will take place. As explained above due to spin blockade this will not be the case for the T(1,1) state. If charge tunneling takes place, a shift in the quantum capacitance (capacitance originating from the DQD charge polarization) will take place, which is read by the gate reflectometry. The probability of finding the DQD system in the T(1,1) state will decay exponentially with the duration of the waiting time tw, with *T*1 being the decay constant, since for long waiting times the DQD will always end in the S(1,1) state.

##### Spin manipulation measurements

Quantum gate operations for a spin qubit system implies spin manipulation. Basically such manipulations are spin rotations in the spin representation sphere, called Bloch sphere.



Figure 10. Bloch sphere

The spin-up and spin-down states form the basis of the hole spin qubit and they are located on the north and south pole of the Bloch sphere. Their energy splitting EZ is determined by the hole g factor g, the Bohr magneton μB and a static external magnetic field B, as . The spin vector precesses around the applied static magnetic field axis with a so-called Larmor frequency , where h is the Planck constant. For flipping the spin an external oscillatory magnetic field BAC needs to be applied perpendicular to the static one and its frequency needs to match the Larmor frequency. An intuitive understanding why the frequency of the BAC needs to match the Larmor frequency can be obtained by thinking of the example of a child on a swing. The child-swing system oscillates with its natural frequency of oscillation. If the swing is pushed by an external person with an appropriate period of pushing pulses, the amplitude of the oscillation will increase and at some point the swing will flip. In this comparison the natural frequency of a child-swing system corresponds to the Larmor frequency and the frequency of the externally applied pushing pulses to the frequency of the applied oscillatory magnetic field.

However, an oscillatory magnetic field is hard to implement, from the fabrication standpoint, since it adds more steps and thus the risk of failure. One way to avoid this problem is to a apply static instead of an oscillatory magnetic field and to apply an oscillatory voltage to the QD gate. The oscillatory electric field can modulate the hole g factor giving thus an equivalent to the first case oscillatory magnetic field. This technique is called g-tensor modulation technique and is going to be used in the qubit I am planning to study.

For generating such high frequency signals, microwave sources are needed because of high Larmor frequencies. For example, expected g factor for holes in Ge is around 3 [10] and standard value of magnetic field is around 0.5 Twhich according to expressions for Ez and f above gives f around 20 GHz. For this purpose a vector signal generator will be used, controlled also from the python measurement application.

###### Measuring the spin dephasing time T2\*

In order to determine coherence times, coherent manipulation of the spin is needed. In order to verify coherent manipulation of the spin, Rabi oscillation experiments will be conducted. The DQD will be initialized in T(1,1) charge configuration. Then the spin in the left dot will be rotated for an angle determined by the spin rotation time τBURST , followed by spin readout by trying to push the DQD to the (0,2) charge configuration (which is a singlet (0,2) configuration as explained already above). If the S(0,2) configuration is achieved, it means that the spin has been rotated. By linearly changing τBURST , a Rabi oscillation pattern [11] should be observed proving the coherent spin manipulation.

Following the approach of R. Maurand et al., for evaluating the inhomogeneous dephasing time T2\*, Ramsey – fringes like experiments will be conducted [11]. First, a ∏/2 pulse around the x axis is applied to bring the spin vector from the north pole (positive z axis) to the xy plane in Figure 10. It stays there for the time τ being exposed to the dephasing noise. After time τ, a second ∏/2 pulse around x axis projects the spin vector back on the z axis for the readout. If no dephasing has taken place, the spin should finish at the south pole of the Bloch sphere (spin up state). Linear increase of the τ between the measurement points results in the exponentially decaying spin up state probability, with T2\* being the dephasing time.

###### Spin coherence time experiments:

1. Spin echo T2ECHO

Coherence can be extended by the so called spin echo technique which can partially cancel dephasing originating for example from slow varying nuclear magnetic field or applied field inhomogeneities. Similar to the spin dephasing time measurement, after the first ∏/2 pulse around the x axis the spin vector lays in the xy plane. Because of the dephasing sources the spin will dephase in the xy plane for time τ. Then a ∏ pulse around the y axis will be applied which mirrors the spin vector around the y axis. The spin is then left to dephase for the same time, but since it is mirrored, the direction of this dephasing will cancel the previous one, causing the so-called spin refocusing. Followed by another ∏/2pulse around x axis, the spin is projected back to the z axis and a spin up probability is measured. From its exponentially decaying envelope in this case the T2ECHO will be extracted.

1. CPMG pulse sequence T2CPMG

Finally, in order to extend further the coherence time we will use the sequence of ∏ pulses called the (CPMG) sequence. The ∏ pulses, rotating the spin around the y axis can be applied at the times τ, 3τ, 5τ…, instead of a single ∏ pulse, as in the spin echo experiment, for the spin refocusing. Coherence time T2CPMG will be extracted from the exponentially decaying envelope of spin up probability vs ∏ pulses separation time τ. This method is insensitive to the ∏ pulse length errors because the rotation axis alternates between y and –y subtracting the pulse length errors [15].

### Innovative aspects of the proposed project:

There has been a huge interest in the past few years in the realization of electron Si spin qubits. In this project a hole spin qubit in a DQD formed in a Ge hut wire will be studied. Despite the interesting electronic properties of this type of nanostructure nothing is known about the spin lifetimes of the confined holes. Due to the low hyperfine interaction and the heavy hole character of the wavefunction very long dephasing times are actually expected [10],[21]. In addition, easy and fast spin state manipulation should be possible because of the in situ present **large spin orbit coupling** for holes in Ge. This will also eliminate the necessity for an oscillatory magnetic field. Such a manipulation by means of oscillatory electric fields in combination with the gate reflectometry will dramatically reduce the fabrication complexity since no extra structures (charge sensor, stripline) are required except of the already defined and necessary gates. Thus this approach has high chances of **addressing the challenge of scalability**.

Finally we aim to achieve the highest reported sensitivity in the gate reflectometry setup. The gates in our DQD system are positioned very closely to the hut wire (less than 4nm – defined simply by the thickness of the dielectric) in which the QDs are formed. This implies **high capacitive coupling between gate and QDs and as a consequence high speed of the gate reflectometry setup** as explained in the *Moving towards gate reflectometry* chapter.

### International collaboration:

We are collaborating with the spin qubit team in the group of C. Marcus in Copenhagen, led by **Ferdinand Kuemmeth (*Since Ferdinand is also my external thesis committee, should I note this here?).*** Actually I have been visiting them for three months end of 2015. Since they are a leading group with a vast knowledge in instrumentation and in the physics of spin dynamics, this collaboration will help me a lot in realizing the proposed project. It would be helpful to visit them once per year to discuss with the technical and physics related questions thus I am requesting 500 Euro ***(What is the reasonable amount that I should put here??)*** per year as travel expenses. The other significant collaboration is with Prof. **J.J. Zhang** who is working in the Chinese Academy of Science, in the Institute of Physics in Beijing, China. He is a material scientist providing us with the very high quality Ge hut wires which very few groups around the world can grow.

### Work table

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **Task** | 1st-6th month | 7th-12th month | 13th-18th month | 19th-24th month | 25th- 31st month | 32nd- 36th month |
| 1. Second generation of the reflectometry setup | X |  |  |  |  |  |
| 1. Moving to the gate reflectometry 2. Optimizing the gate reflectometry |  | X |  |  |  |  |
| 1. Measuring the spin relaxation time T1 |  |  | X |  |  |  |
| 1. Determining the various spin coherence times |  |  |  | X | X | X |

After each successful experiment a publication will be submitted to a high impact factor journal.

### Contingency plan:

In case it turns out that the gate reflectometry technique is not sensitive/fast enough we are going to use ohmic reflectometry. For that reason a charge sensor proximate to the double QD should be added during the nanofabrication process of the samples. Charge sensing has been recently demonstrated in our group for hut wires [22]. For the charge sensor a single QD located very closely and capacitively coupled to the DQD is going to be used. Whenever the charge configuration in the DQD will change, the impedance of the charge sensor will change and thus the reflected signal amplitude.

### Personal qualification

I performed my undergraduate studies at the faculty of electrical and computer engineering, at the University of Zagreb, Croatia. During my undergraduate studies I was a teaching assistant in the course “Electronics” which is the mandatory course for all students on the faculty. For my bachelor thesis I have been measuring ECL ring oscillators based on horizontal current transistor (HCBT). This allowed me to deepen my knowledge in electronic instrumentation. For my master thesis, performed with the professor Tomislav Suligoj, I have focused on design and analysis of the RF circuits in 180 nm BiCMOS technology with the HCBT, which gave me a background in performing simulations, design and analysis of the electronics circuits.

Fascinated by the idea of quantum computation, I moved in April to the Johannes Kepler University to work as a research assistant in the group of dr.sc. Georgios Katsaros. There I started working on the development of an ohmic reflectometry system for charge readout of SiGe QDs. The realization of printed circuit board designs, the development of python codes for controlling various DC and high frequency signal instruments were among my tasks. I also performed 4K measurements on single hole transistors based on SiGe nanowire QDs fabricated in our group by Hannes Watzinger. During that time I had the chance to attend also an important conference in the field: SpinTech VIII in Basel, Switzerland, 10-13 August 2015. In October 2015, and for three months, I went on a research visit to the Center for Quantum Devices, Niels Bohr Institute, Copenhagen. I worked in the group of Ferdinand Kuemmeth. This group is developing spin based qubits in GaAs and Si/SiGe lithographically defined double and triple QDs. They are one of the biggest and most successful groups in the field of quantum computation. During my research stay, I learned about high end laboratory equipment including cryogen free dilution refrigerators, waveform and signal generators, RF equipment (amplifiers, filters, special type of coaxial cables… ). I was also following the experiment of Filip Malinowski – tuning the GaAs double and triple QD for coherent spin manipulation and readout using a charge sensor ohmic reflectometry setup. Since 2016 I am a PhD student of the professor Georgios Katsaros, at the Institute of Science and Technology (IST), Austria, currently working on a second version of a reflectometry readout system for spin relaxation experiments.

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